APPLICATION FOR U.S. PATENT TRANSMITTAL FORM

Docket No. TI-19177

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Assistant Commissioner
for Patents
Washington, DC 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventors: Robert Alvarez, Paul r. Moehle, and Harold T. Kelleher

For: STABILIZER/SPACE FOR SEMICONDUCTOR DEVICE

Enclosed are:

PTO Form 1595 and Assignment of the invention to TEXAS INSTRUMENTS INCORPORATED
9 pages of Specification
5 sheets of formal drawings.
A Declaration/Power of Attorney

Please amend the specification by inserting the following before the first line:

This application claims priority under 35 USC § 119(e)(1) of provisional application number **60/032,500** filed 11/27/96

FEE CALCULATION					FEE
	NUMBER		NUMBER EXTRA	RATE	BASIC FEE $790.00
Total Claims	14	- 20	0	x $22 =	-0-
Independent Claims	3	-3	0	x $82 =	-0-
				Total Filing Fee	$790.00

Please charge Deposit Account No. 20-0668 in the amount of the Total Fees set forth. The Assistant Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 20-0668. An original and two copies of this form are submitted.

All correspondence related to this application may be addressed to the undersigned at Texas Instruments Incorporation, P.O. Box 655474, M/S 219, Dallas, Texas 75265.

11/5/97
Date

W. James Brady III
Attorney for Applicant(s)
Registration No. 32,080

STABILIZER/SPACER FOR SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

This invention relates to semiconductor devices, and more particularly to a ceramic or plastic stabilizer/spacer for devices having high pin count lead frames.

BACKGROUND OF THE INVENTION

In producing delicate, high pin count lead frames with closely spaced inner leads, polyimide or kapton tape is often applied to maintain lead-to-lead spacing and to stabilize lead tip planarity. This operation is typically done after stamping or etching the lead frame and after plating of the lead frame. It involves indexing and precisely locating a lead frame unit and applying heat and pressure to a piece of precisely cut and located polyimide tape to affix it to the lead frame. This operation is expensive, time consuming and subjects the high value added plated lead frame to additional mechanical handling. Ionic contamination is often found in polyimide taped lead frames.

BRIEF SUMMARY OF THE INVENTION

The invention is a leadframe/stabilizer for use with semiconductor devices. The stabilizer is for stabilizing the space between lead frame leads and improving the lead to lead spacing, and to improve lead tip planarity. The stabilizer extends partially along the length of and on each side of said lead frame leads and a die pad mount, integral with and forming a part of said stabilizer, is mounted where the die mount pad of a lead frame would be.

The technical advance represented by the invention, as well as the objects thereof, will become apparent from the following description of a preferred embodiment of the invention when considered in conjunction with the accompanying drawings, and the novel features set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a fixture and lead frame illustrating the use of a punch and die to place a prior art polyimide tape on the leads;

Fig. 2 illustrates a single lead frame with the polyimide stabilizer in place;

Fig. 3 is a cross-sectional view of the polyimide stabilizer/spacer on the leads;

Fig. 4 is a lead frame strip of two stabilized lead frames according to the present invention;

Fig. 5 shows a single lead frame;

Fig. 6 shows a lead frame removed from the lead frame strip.

DESCRIPTION OF A PREFERRED EMBODIMENT

Figs. 1, 2 and 3 illustrate a prior art method for providing a stabilizer spacer for lead frame leads in high pin count lead frames. A lead frame 10 having index holes 13 is placed on a heater block 11 having indexing pins 12 hold the lead frame in place on the block. A die 17 having die holes 20 is placed over lead frame 10 such that the die holes 20 span leads 15. A sheet of polyimide 18 is placed over the die and a punch having punch elements 19 corresponding to the openings 20 in die 17 is placed over the polyimide. Punch elements 19 punch small strips of polyimide material out of sheet 18 onto leads 15. Fig. 2 shows the strips 25 of polyimide on leads 15 after the strips 25 have been punched out of sheet 18. Fig. 3 is a cross sectional view of polyimide strips 25 and leads 15. Heat from a heater block supplies heat to aid in the adhesion of strips 25 to leads 15.

Fig. 4 shows a lead frame strip 30 having two lead frames 33 and 34. Usually a strip of lead frames has more than two lead frames, but for purpose of illustration, only two lead frames are illustrated. Each lead frame has a plurality of sets of lead frame leads on each side, for example, sets shown as 36, 37, 38 and 39. While three lead frame lead are shown on each side, there usually

are many more leads, and the number of leads depends upon the particular semiconductor device to be the mounted within the lead frame. The lead frames in lead frame strip 30 are held together by side and cross rails 31.

A die pad/lead frame lead stabilizer 35 is molded such that a portion of the stabilizer 35 extends between the lead frame leads and forms a die pad area 40 on which the semiconductor die is mounted. The stabilizer material may extend up to, for example 50% of the lead frame length, but the length of extension between the lead frame leads may depend upon the length of the lead frame leads.

Area 40 may be a recessed area as shown, or may be a flat non-recessed area. Stabilizer 35 is of a suitable plastic material such as molding compounds used in encapsulating semiconductor devices or a ceramic compound. Utilization of a non-metal material for the die pad mount may be important in some devices, since in some integrated circuit devices, chip-to-metal mounting of the semiconductor die on a metal die mount pad causes movement of the semiconductor die with respect to the die mount pad because of thermal expansion of the metal die pad.

Fig. 5 shows a single lead frame 30a after separation from the strip 30 of lead frames. Lead frame 30a still has part of the lead

frame 31 holding the ends of the lead frame leads 36-39 together. Since stabilizer 35 holds lead sets 36-39 in place with the stabilizer fingers 35a, lead sets 36-39 may be separated by the removal of the joining parts of lead frame 31.

Fig. 6 shows the lead frame 30a after the lead frame rails 31 have been removed. The individual leads 36-39 are held in place by the stabilizer fingers 35a. Stabilizer 35 holds the leads in place adjacent the die mount pad area 40.

Stabilizer 35 improves lead-to-lead spacing since the leads are held in place by stabilizer 35. Stabilizer 35 eliminates the need to introduce foreign contaminants such as plastic tape and adhesives that are used as lead stabilizers. Also eliminated in most devices is the need for a die pad mount since stabilizer 35 incorporates a die pad mount into the stabilizer.

An additional feature is the improved adhesion of package mold compound to the mold compound material of stabilizer 35. There is improvement in the relative thermal movement between the semiconductor chip and die mount pad since mold compound replaces the standard metal die pad of most lead frames.

WHAT IS CLAIMED

1. A leadframe/stabilizer for use with semiconductor devices, comprising:

a plurality of lead frame leads;

a stabilizer extending partially along the length of and on each side of said lead frame leads; and

a die pad mount integral with and forming a part of said stabilizer.

2. The leadframe/stabilizer according to Claim 1, wherein said stabilizer is made of an insulating material.

3. The leadframe/stabilizer according to Claim 1, wherein said stabilizer is made of a plastic material.

4. The leadframe/stabilizer according to Claim 1, wherein said stabilizer is made of a ceramic material.

5. The leadframe/stabilizer according to Claim 1, wherein said die pad mount has a recess in one surface into which a semiconductor die is mounted.

6. A leadframe/stabilizer for use with semiconductor devices, comprising:

a plurality of lead frame leads;

a stabilizer extending partially along the length of and on each side of said lead frame leads;

a die pad mount integral with and forming a part of said stabilizer; and

a recess in one surface of the die pad mount into which a semiconductor die is mounted

7. The leadframe/stabilizer according to Claim 6, wherein said stabilizer is made of an insulating material.

8. The leadframe/stabilizer according to Claim 6, wherein said stabilizer is made of a plastic material.

9. The leadframe/stabilizer according to Claim 6, wherein said stabilizer is made of a ceramic material.

10. A method for stabilizing the leads of a lead frame and providing a semiconductor die mount pad, comprising the steps of:

molding a stabilizer fingers along part of the length and on each side of the lead frame leads;

molding a die pad integral with the stabilizer fingers.

11. The method according to claim 10, including the step of forming a recessed area in the die pad for mounting of a semiconductor die.

12. The method according to Claim 10, wherein said stabilizer is made of an insulating material.

13. The method according to Claim 10, wherein said stabilizer is made of a plastic material.

14. The method according to Claim 10, wherein said stabilizer is made of a ceramic material.

ABSTRACT OF THE DISCLOSURE

The invention is a leadframe/stabilizer (35) for use with semiconductor devices. Stabilizer (35) is for stabilizing the space between of lead frame leads (36-39) and improving the lead to lead spacing and to improve lead tip planarity. Stabilizer (35) extends partially along the length of and on each side of said lead frame leads (36-39) and include a die pad mount (40), integral with and forming a part of said stabilizer 35.

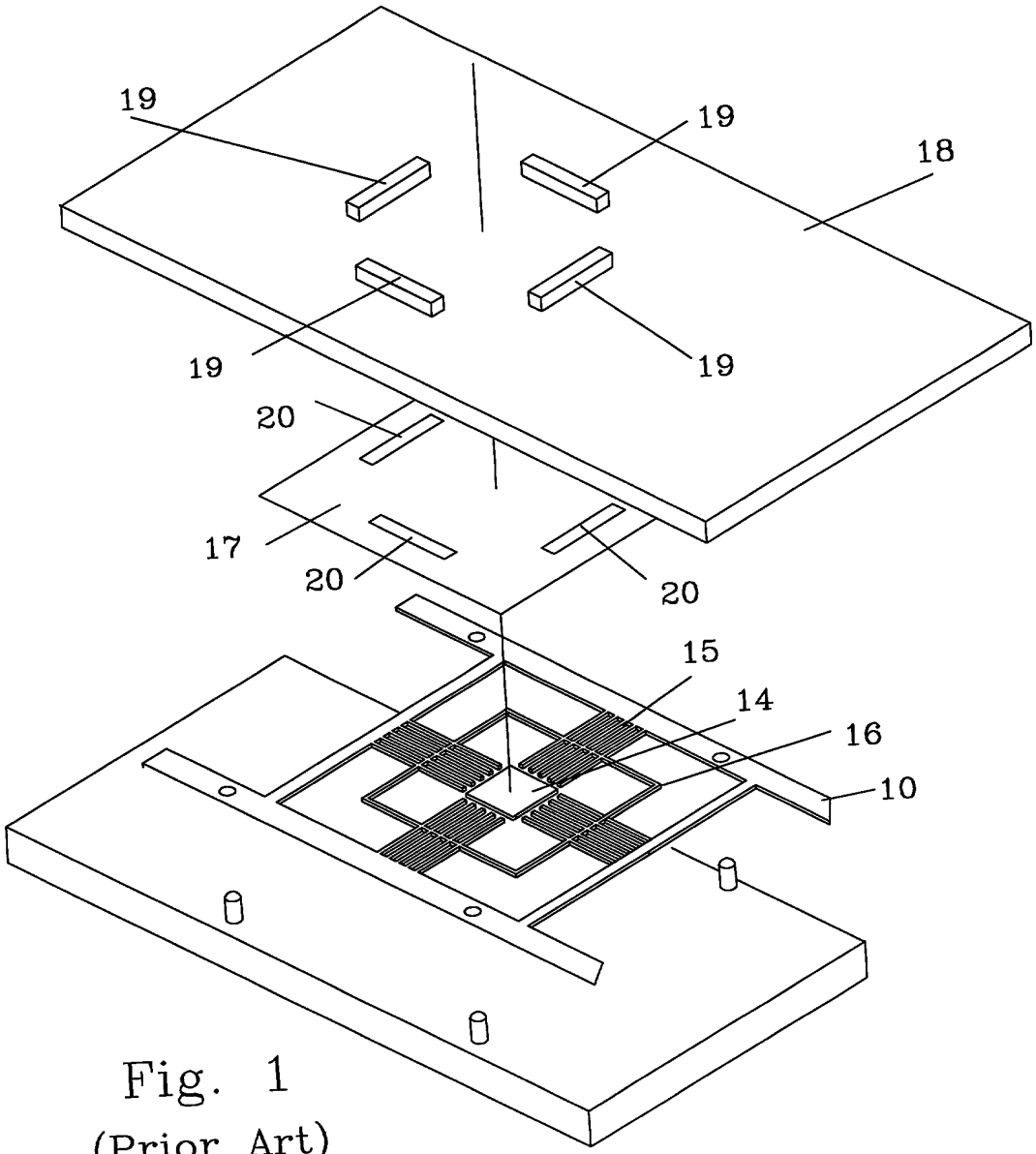

Fig. 1
(Prior Art)

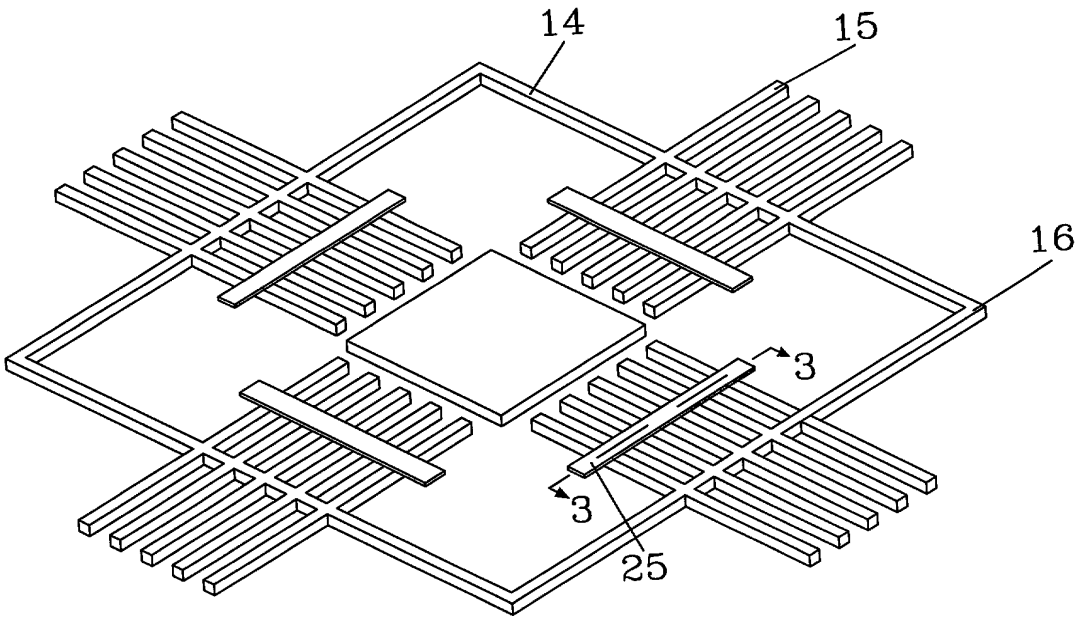

Fig. 2
(Prior Art)

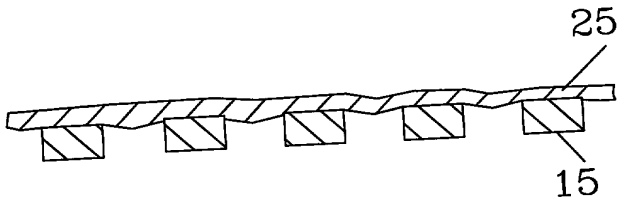

Fig. 3
(Prior Art)

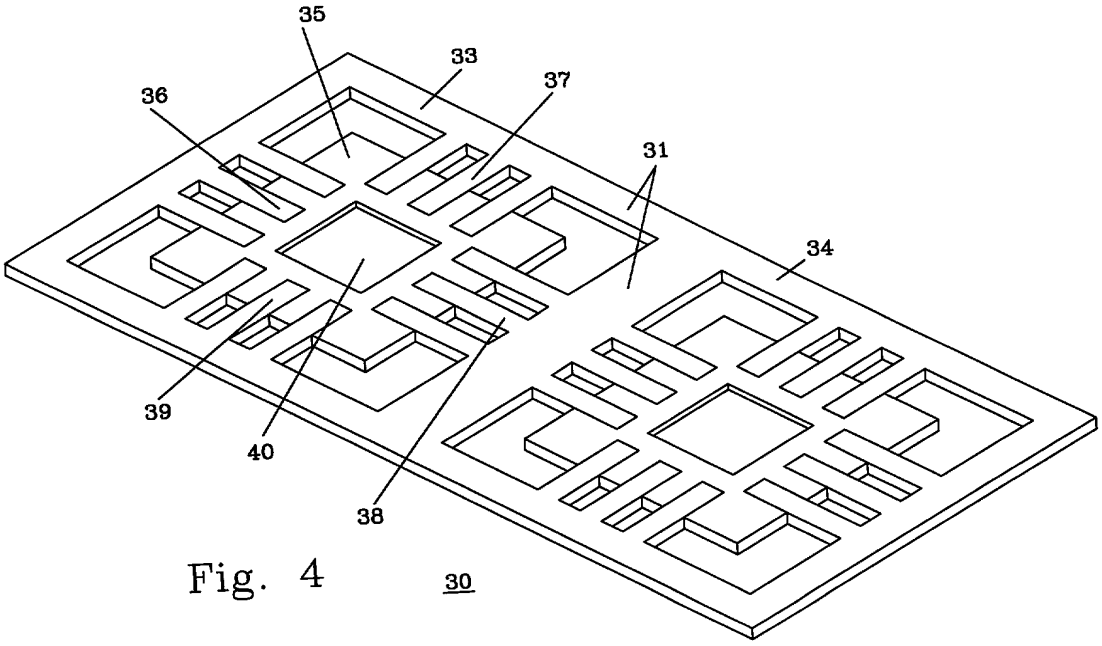

Fig. 4 30

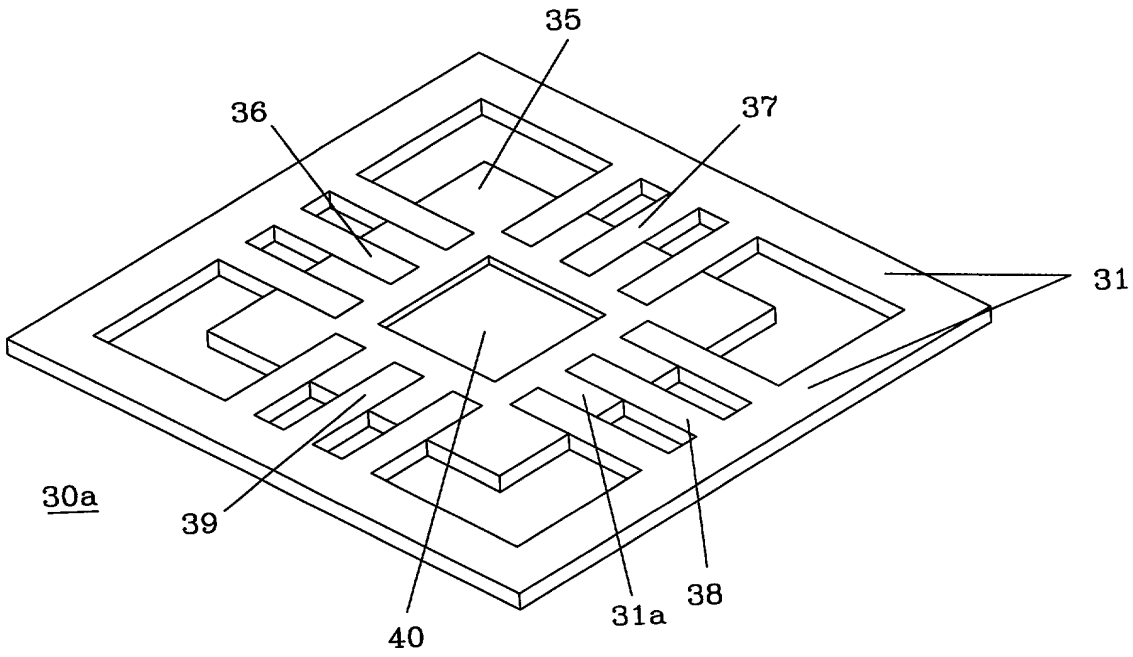

Fig. 5

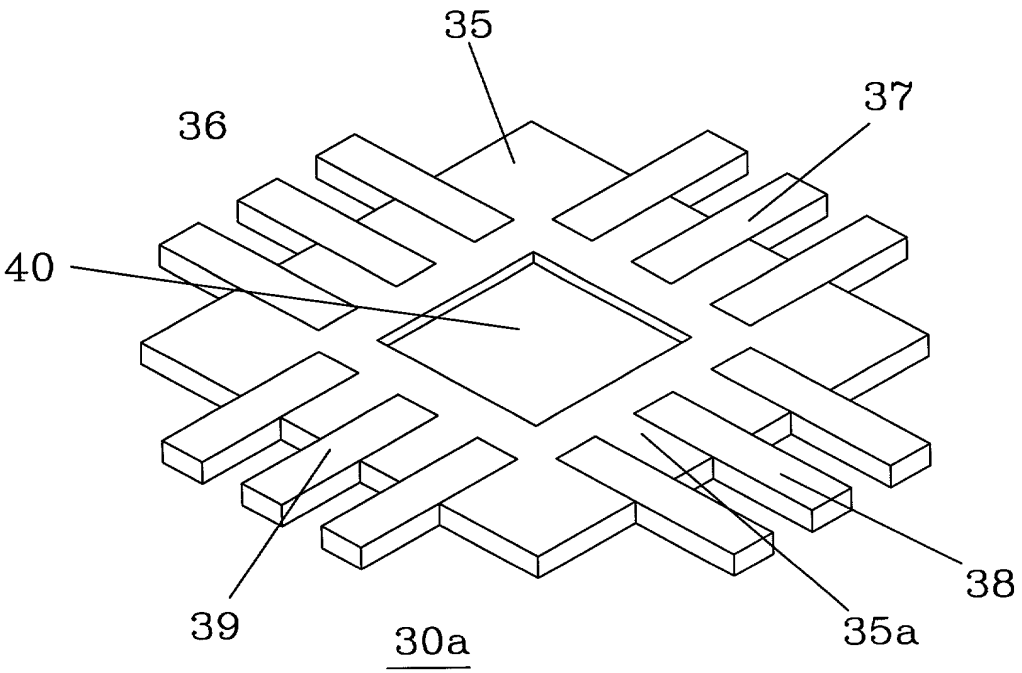

Fig. 6

ATTORNEY'S DOCKET NO
TI19177

APPLICATION FOR UNITED STATES PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, section 1.56(a);

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code. and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION
STABILIZER/SPACER FOR SEMICONDUCTOR DEVICE

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

Wade James Brady, III, Reg. No. 32,080
Richard Donaldson, Reg. No. 25,673
John E. Vandigriff, Reg. No. 22,127
Jay M. Cantor, Reg. No. 19,906

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
Wade James Brady, III Texas Instruments Incorporated Patent Department M.S. 219 P.O. Box 65547 Dallas, Texas 75265	(917) 995-1355

NAME OF INVENTOR: (1)	NAME OF INVENTOR. (2)	NAME OF INVENTOR: (3)
Robert Alvarez	Paul R. Moehle	Harold T. Kellher
RESIDENCE & POST OFFICE ADDRESS: 310 Wildbriar Dr. Garland, Tx 75043	RESIDENCE & POST OFFICE ADDRESS 221 Walker St. Seekonk, MA 02991	RESIDENCE & POST OFFICE ADDRESS: 389 South Main St. Attleboro, MA 02103
COUNTRY OF CITIZENSHIP: U.S.A.	COUNTRY OF CITIZENSHIP: U.S.A.	COUNTRY OF CITIZENSHIP: U.S.A.
SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE: 6/6/97	DATE: 6/2/97	DATE: 6/2/97